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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : David Lewis et al.
Application No. : 10/766,464
Confirmation No. : 3178
Filed : January 27, 2004
For : ERROR CORRECTION FOR PROGRAMMABLE
LOGIC INTEGRATED CIRCUITS
Art Unit : 2113
Examiner : Robert W. Beausoliel, Jr.

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

New York, New York 10020
March 10, 2006

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97,
applicants hereby make the following references of record
in the above-identified patent application:

U.S. Patent Documents

4,005,405	West	01/25/1977
4,375,664	Kim	03/01/1983
4,866,717	Murai et al.	09/12/1989
5,111,464	Farmwald et al.	05/05/1992
5,305,324	Demos	04/19/1994
5,495,491	Snowden et al.	02/27/1996
5,511,211	Akao et al.	04/23/1996
5,581,198	Trimberger	12/03/1996
5,588,112	Dearth et al.	12/24/1996

U.S. Patent Documents

5,754,566	Christopherson et al.	05/19/1998
5,978,952	Hayek et al.	11/02/1999
6,024,486	Olarig et al.	02/15/2000
6,065,146	Bosshart	05/16/2000
6,101,614	Gonzales et al.	08/08/2000
6,223,309	Dixon et al.	04/24/2001
6,279,128	Arnold et al.	08/21/2001
6,349,390	Dell et al.	02/19/2002
6,701,480	Karpuszka et al.	03/02/2004
6,832,340	Larson et al.	12/14/2004
6,838,899	Plants	01/04/2005
6,839,868	Pignol	01/04/2005
6,847,554	Satori	01/25/2005
6,848,063	Rodeheffer et al.	01/25/2005
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7,007,203	Gorday et al.	02/28/2006

U.S. Published Documents

2004/0230767	Bland et al.	11/18/2004
2005/0040844	Plants	02/24/2005
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2005/0073884	Gonzalez et al.	04/07/2005
2005/0144551	Nahas	06/30/2005
2005/0154943	Alexander et al.	07/14/2005

Foreign Patent Documents

JP 61101857 (Abstract)	Japan	05/20/1986
JP 62251949 (Abstract)	Japan	11/02/1987
WO 98/29811	PCT	07/09/1998
EP 1 100 020	EPO	05/16/2001

Non-Patent Documents

Bazes et al., "Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-port Memory and Error Checking and Correction," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 2, April 1983, Abstract.

Ahrens et al., "Predictive Maintenance for Prevention of Uncorrectable Multiple BIT Errors in MEMORY," IP.com, Prior Art Database, January 28, 2005, pp. 1-5 (originally published: IBM TDB, August 1, 1989, pp. 239-244).

Matsumoto, "Million-gate architecture will vie with ASIC-like approach from Altera, Lucent and GateField - size matters, says Xilinx with Virtex launch," Electronic Engineering Times, October 26, 1998.

Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Transactions on Computers, Vol. 37, No. 2, February 1998, Abstract.

Michinishi et al., "Testing for the programming circuit of SRAM-based FPGAs," IEICE Transactions on Information and Systems, Vol. E82-D, No. 6, 1999, Abstract.

Wang et al., "SRAM Based Re-programmable FPGA for Space Applications," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pp. 1728-1735.

Huang et al., "A memory coherence technique for online transient error recovery of FPGA configurations," Proceedings of the 2001 ACM/SIGDA 9th International Symposium on Field Programmable Gate Arrays, February 11-13, 2001, pp. 183-192.

"Antifuse FPGA shoots for the stars," EDN, Vol. 48, No. 12, May 29, 2003, p. 20.

Johnson, "Multibit error correction in a monolithic semiconductor memory," IP.com Prior Art Database, September 8, 2003, pp. 1-10.

"Tradeoffs abound in FPGA design: understanding device types and design flows is key to getting the most out of FPGAs," Electronic Design, Vol. 51, No. 27, December 4, 2003, p. S1.

Tiwari et al., "Enhanced Reliability of Finite-State Machines in FPGA Through Efficient Fault Detection and Correction," IEEE Transactions on Reliability, Vol. 54, No. 3, September 2005, pp. 459-467.

The aforementioned documents are listed on the accompanying Form PTO/SB/08 (submitted in duplicate). Pursuant to 37 C.F.R. § 1.98(a)(2), copies of the U.S. Patent Documents and U.S. Published Documents are not provided. Copies of the Foreign Patent Documents and Non-Patent Documents are submitted herewith.

Applicants request that a copy of Form PTO/SB/08, as considered and initialed by the Examiner, be returned with the next communication.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully submitted,

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

MAR 10 2006

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Sheet 1 of 4

Application Number	10/766,464
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Examiner Name	Robert W. Beausoliel
Attorney Docket Number	174/285
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U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		4,005,405	01/25/1977	West	
		4,375,664	03/01/1983	Kim	
		4,866,717	09/12/1989	Murai et al.	
		5,111,464	05/05/1992	Farmwald et al.	
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		5,495,491	02/27/1996	Snowden et al.	
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		6,223,309	04/24/2001	Dixon et al.	
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		6,701,480	03/02/2004	Karpuszka et al.	
		6,832,340	12/14/2004	Larson et al.	
		6,838,899	01/04/2005	Plants	
		6,839,868	01/04/2005	Pignol	
		6,847,554	01/25/2005	Satori	

Examiner
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Considered

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		6,848,063	01/25/2005	Rodeheffer et al.	
		6,859,904	02/22/2005	Kocol et al.	
		7,007,203	02/28/2006	Gorday et al.	

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		2004/0230767	11/18/2004	Bland et al.	
		2005/0040844	02/24/2005	Plants	
		2005/0044467	02/24/2005	Leung et al.	
		2005/0073884	04/07/2005	Gonzalez et al.	
		2005/0144551	06/30/2005	Nahas	
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FOREIGN PATENT DOCUMENTS

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		JP 61101857 (Abstract)	05/20/1986	Hitachi Ltd.		
		JP 62251949 (Abstract)	11/02/1987	Mitsubishi Electric Corp.		
		WO 98/29811	07/09/1998	Intel Corp.		
		EP 1 100 020	05/16/2001	Matsushita Electric Ind. Co., Ltd.		

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NON PATENT LITERATURE DOCUMENTS

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		Bazes et al., "Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-port Memory and Error Checking and Correction," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 2, April 1983, Abstract.
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		Matsumoto, "Million-gate architecture will vie with ASIC-like approach from Altera, Lucent and GateField – size matters, says Xilinx with Virtex launch," Electronic Engineering Times, October 26, 1998.
		Mahmood et al., "Concurrent Error Detection Using Watchdog Processors – A Survey," IEEE Transactions on Computers, Vol. 37, No. 2, February 1998, Abstract.
		Michinishi et al., "Testing for the programming circuit of SRAM-based FPGAs," IEICE Transactions on Information and Systems, Vol. E82-D, No. 6, 1999, Abstract.
		Wang et al., "SRAM Based Re-programmable FPGA for Space Applications," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pp. 1728-1735.
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